

AMENDMENTS IN THE SPECIFICATION

Please replace the paragraph beginning on page 13, line 27 with the following:

In the heterogeneous data processing system, the heterogeneity typically extends to the processor's micro architectures, i.e., the execution blocks of the processor, the FXU, FPU, ISU, LSU, IDUs, etc., are designed to support the operational characteristics associated with the processor. Additionally, heterogeneity also extends to the cache topology including different cache levels, cache states, cache sizes, and shared caches. Heterogeneity would necessarily extend to the memory controllers micro-architecture and memory frequency and the I/O controller micro-architecture and I/O frequencies. Also heterogeneity supports processors operating with in-order execution, some out-of-order execution, or robust (*i.e., complete and reliable*) out-of-order execution.